Amendments to the Claims

Claim 1–9 (canceled)

Claim 10 (Currently amended). A digital-analog converter having:

a) an array arrangement having a number of cells between a first and a last cell configured to output at least one quantized analog signal, the cells having a local decoder device configured to receive two row actuation signals and three column actuation signals;

b) a dynamic element matching (DEM) logic device configured to generate at least one arithmetic sign signal and two digital output data items from digital input data on the basis of a predetermined DEM algorithm in order to determine an initial cell and a final cell in the array ~~cells~~ arrangement having energy sources which are to be activated, the at least one arithmetic sign signal determining whether cells adjoining the first cell in the array arrangement are activated if the cells to be activated reach the last cell in the array arrangement; and

c) a decoder device configured to decode ~~the at least to digital output data items and~~ the at least one arithmetic sign signal and two digital output data items from the DEM device into the two row actuation signals and three column actuation signals, which are coupled to the array arrangement for the purpose of activating energy sources for the cells which are to be activated.

Claim 11 (Previously presented). The digital-analog converter as claimed in claim 10, wherein the array arrangement has single cells with a respective current source as the energy source.

Claim 12 (Previously presented). The digital-analog converter as claimed in claim 10, wherein the DEM logic device has a parallel input for supply the digital input data, which has a predetermined bit length.

Claim 13 (Previously presented). The digital-analog converter as claimed in claim 10, wherein the decoder device is further configured to generate two complementary row actuation signals and three complementary column actuation signals which are coupled to the array arrangement for the purpose of activating energy sources for predetermined cells.

Claim 14 (Previously presented). The digital-analog converter as claimed in claim 10, wherein the array arrangement is configured to generate two mutually inverse quantized analog output signals.

Claim 15 (Previously presented). The digital-analog converter as claimed in claim 10, wherein an input of a respective local decoder device is adapted to receive two complementary row actuation signals and three complementary column actuation signals.

Claim 16 (Currently amended). The digital-analog converter as claimed in claim 10, wherein the local decoder device respectively connects an energy source to a resistor when a first column signal and a first row signal, or second column signal and a second ~~rwo~~ row signal, or a third column signal, are activated.

Claim 17 (Previously presented). The digital-analog converter as claimed in claim 10, wherein the array arrangement has a respective edge length of at least 64 cells corresponding to a bit length for the input signal of at least 12 bits.

Claim 18 (Previously presented). The digital-analog converter as claimed in claim 10, wherein the DEM logic device is configured to generate the at least one arithmetic sign signal and two digital output items on the basis of one of a group of DEM algorithms comprising a data weighted averaging algorithm, a bidirectional data weighted averaging algorithm, and an individual level averaging algorithm.

Claim 19 (Currently amended). A digital-analog converter having:

a) an array arrangement having a number of cells between a first and a last cell configured to output at least one quantized analog signal, the cells having a local decoder device configured to receive row actuation signals and column actuation signals;

b) a dynamic element matching (DEM) logic device configured to generate at least one arithmetic sign signal and two digital output data items from digital input data on the basis of a predetermined DEM algorithm in order to determine an initial cell and a final cell in the array ~~cells~~ arrangement having energy sources which are to be activated, the at least one arithmetic sign signal determining whether cells adjoining the first cell in the array cells are activated if the cells to be activated reach the last cell in the array arrangement; and

c) a decoder device configured to decode the at least ~~to digital output data items and the~~ one arithmetic sign signal and two digital output data items from the DEM device into the row actuation signals and column actuation signals, which are coupled to the array arrangement for the purpose of activating energy sources for the cells which are to be activated.

Claim 20 (Previously presented). The digital-analog converter as claimed in claim 19, wherein the array arrangement has single cells with a respective current source as the energy source.

Claim 21 (Previously presented). The digital-analog converter as claimed in claim 19, wherein the decoder device is further configured to generate complementary row actuation signals and complementary column actuation signals which are coupled to the array arrangement for the purpose of activating energy sources for predetermined cells.

Claim 22 (Previously presented). The digital-analog converter as claimed in claim 19, wherein the array arrangement is configured to generate two mutually inverse quantized analog output signals.

Claim 23 (Previously presented). The digital-analog converter as claimed in claim 19, wherein an input of a respective local decoder device is adapted to receive complementary row actuation signals and complementary column actuation signals.

Claim 24 (Previously presented). The digital-analog converter as claimed in claim 19, wherein the local decoder device respectively connects an energy source to a resistor responsive to a particular combination of a row actuation signal and a column actuation signal, or responsive to a particular column actuation signal independent of any row actuation signal.

Claim 25 (Previously presented). The digital-analog converter as claimed in claim 19, wherein the DEM logic device is configured to generate the at least one arithmetic sign signal and two digital output items on the basis of one of a group of DEM algorithms comprising a data weighted averaging algorithm, a bidirectional data weighted averaging algorithm, and an individual level averaging algorithm.

Claim 26 (Currently amended). A digital-analog converter having:

a) an array arrangement having a number of cells between a first and a last cell configured to output at least one quantized analog signal, the cells having a local decoder device configured to receive row actuation signals and column actuation signals; and

b) a control circuit configured to generis the row actuation signals and the column actuation signals, which are coupled to the array arrangement for the purpose of activating energy sources for the cells which are to be activated, the row actuation signals and the column actuation signals configured to cause the array arrangement to activate energy sources of a set of cells defined by an initial cell and a final cell, the initial cell and final cell determined on the basis of a predetermined dynamic element matching (DEM) algorithm.

Claim 27 (Previously presented). The digital-analog converter as claimed in claim 26, wherein the local decoder circuit is configured to receive two row activation signals and three column activation signals.

Claim 28 (Previously presented). The digital-analog converter as claimed in claim 27, wherein the control circuit comprises a logic device and a decoder device, the logic device operable to generate two data items indicative of the initial cell and the final cell, and the decoder device operable to generate the two row activation signals and the three column activation signals based on at least the two data items.

Claim 29 (Previously presented). The digital-analog converter as claimed in claim 26, wherein the control circuit is configured to determine the initial cell and the final cell on the basis of one of a group of DEM algorithms comprising a data weighted averaging algorithm, a bidirectional data weighted averaging algorithm, and an individual level averaging algorithm.